Modified Dual Active Bridge DC/DC Converter with Improved Efficiency and Interoperability in Hybrid LCC/VSC HVDC Transmission Grids

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***Abstract*- DC transmission grids are the promising electrical networks in the near future especially with the high penetration of large scale renewables. This paper proposes a modified version of the dual active bridge (DAB) DC/DC converter with AC link capacitors generating reactive power to compensate for non-active power consumption; hence mitigating current stresses and losses to improve efficiency. The proposed topology also enables the connectivity of current source line-commutated HVDC and voltage source HVDC technologies particularly during power reversal; a feature which conventional DAB is incapable of doing. Analysis and detailed design of the proposed converter are addressed and a comparative performance analysis is carried out with conventional DAB. Converter principle of operation is explained and Matlab/Simulink simulations are carried out to verify converter operation particularly under adverse conditions such as rated power reversal and DC fault conditions. A low scale prototype substantiates the theoretical analysis and simulation results.**

***Index terms*- DC/DC converter, dual active bridge (DAB), hybrid HVDC grids, line commutated converter (LCC), voltage source converter (VSC).**

I. INTRODUCTION

DC/DC converters are becoming increasingly important in HVDC transmission grids primarily acting as their AC transformer counterpart in AC grids interconnecting DC lines with different DC voltage levels [1]. However, with the growing need to shift from point-to-point transmission to meshed DC grids, DC/DC converters are demonstrating other attractive characteristics that will solve several challenges facing this transition [2]. Such challenges include the absence of reliable high voltage DC circuit breakers, the potential need for interface of current source and voltage source HVDC technologies (particularly during power reversal) and power flow control difficulty. Recent research in high power DC/DC converters has shown promising solutions for these challenges [3-5].

A megawatt-size thyristor-based DC/DC converter has been proposed in [6]. This converter is capable of achieving moderate stepping ratio with inherent fault isolation characteristics. However, it suffers from low switch utilization, low efficiency at high stepping ratio, uncontrollable reactive power and rating of both LV and HV side semiconductors at HV level. An IGBT-based DC/DC converter utilizing DAB topology with an LCL AC link circuit was proposed in [7] to overcome some of the drawbacks in [6] and to enable higher voltage stepping ratios. With IGBTs, higher frequency is possible compared to thyristors leading to an overall reduction in passive elements footprint. Nevertheless, this converter has no isolating transformer and does not enable interface of LCC-based HVDC systems. In [8-15], two-level converter and MMC-based versions of the conventional front-to-front DAB DC/DC converter are presented for various applications. Multilevel based versions include hybrid versions such as controlled transition bridge converter [3], transition arm multilevel converter [14], alternate arm converter [15], quasi two-level converter [16] and cascaded two-level converter [3]. An isolating transformer is used to achieve voltage stepping and galvanic isolation. However, the topologies are not suitable for interfacing LCC-based HVDC links and non-active power circulation in the AC link is unavoidable due to the magnetic requirements of the isolating transformer; hence increased RMS AC link current and losses. DC-MMC [17] has been proposed for connection of multiple low voltage photovoltaics through low power DAB modules. These are interfaced to HVDC link using series-stacked MMC submodules (SMs). Although this topology provides several favourable features such as low component count, modularity, faulty module bypass and absence of bulky high frequency transformer, however, it does not provide LCC/VSC interoperability and the topology would get overcomplicated if handling bi-directional power flow between two HVDC sides. This is because there will be a need to stack low power DABs in series/parallel at input and/or output sides (IS/IP/OS/OP) to realize connection to HVDC.

Some DC/DC converters suitable for hybrid LCC/VSC HVDC grids have been proposed in literature. The thyristor-based active-forced-commutated bridge DC transformer [18] utilizes thyristors allowing low conduction losses. However, an auxiliary self-commutated full bridge (FB) chain-link circuit of N series connected FB MMC SMs is added. Also in order to create the FB chain links, DC link capacitors are required. Although the main power flow control is similar to classical DAB, a huge number of component is required and careful switching between transition states is required. The DC-DC auto-

transformer [19] utilizes three VSCs in series and three AC transformers in parallel to realize the interconnection between LCC and VSC systems, which overcomplicates its design and operation, yet it does not cater for negative DC voltage operation on LCC side in case of swap of rectification and inversion modes.

In this paper, a modified version of the DAB DC/DC converter is proposed for high power DC transmission grids. This is driven by the additional needs, not (or partially) met by the current topologies, namely; lower losses/higher efficiency and capability of integrating LCC-based HVDC systems with VSC-based systems for future multi-terminal networks. The proposed modified DAB is an extension of conventional three phase and single phase DAB incorporating internal AC capacitors to regulate the transfer of power across the HF transformer. The modification maintains the advantages of conventional DAB while enabling operation with improved efficiency and interoperability in hybrid LCC/VSC grids. MMC topology variant of the converter can be also realized.

The idea for the proposed modification in DAB topology stemmed from the fact that to improve efficiency, the AC inductive link RMS current needs to be reduced. To achieve this, the AC inductive link needs to experience higher effective voltages from the two bridges (for the same DC link voltages) to reduce RMS current for the same power transferred. To achieve this required voltage boost, AC capacitors are placed at the bridge outputs and the two bridges are converted to operate in current source mode with bi-directional switching devices and DC side inductor as depicted in Fig.1. This arrangement yields manifold benefits:

1. The peak/RMS voltages across the AC capacitors will be boosted compared to DC link enabling RMS current reduction, hence improved efficiency and reduced IGBT current ratings. Amount of RMS current reduction will be one of the design factors of the proposed converter.
2. The reactive power generated by the capacitors could fully or partially compensate the absorbed reactive power by the inductive link. Zero reactive power operation is possible at rated power which also contributes to RMS and peak current reduction.
3. Zero reactive power (unity power factor) also ensures zero current switching (ZCS) operation of the switching devices at rated power. This minimizes switching losses and simple lossless snubbers would be sufficient.
4. The current source topology of the bridges provides a natural interface to LCC HVDC technology unlike conventional DAB which does not enable reverse DC voltage polarity. Interface with VSC HVDC is also possible.

The aforementioned benefits represent the main contributions of this modified DAB topology, which also inherits the following characteristics of conventional DAB:

- Use of medium frequency transformer to allow galvanic isolation and high voltage step ratios.
- Inherent natural isolation of DC side faults [20-21]. This is highly advantageous in all DAB-based topologies as it implies no control action is necessary to block/trip active semiconductor switches to protect converter from short circuit overcurrents.
- Possibility of regulating power in meshed DC grid transmission lines.

The remaining part of this paper is organized as follows. Section II presents the proposed DC/DC converter topology, steady state analysis and procedure for calculation of passive elements. In section III, the converter design procedure and performance analysis are detailed. Section IV presents Matlab/Simulink simulations to show the proposed converter performance under different operating scenarios including power reversal and DC faults while interfacing two VSCs at different DC voltage levels in addition to interfacing LCC with VSC. The simulation also compares performance with conventional DAB to verify efficiency improvement which the proposed topology introduces. A lab-scale prototype is implemented to validate the simulation results, and this is presented in section V. Section VI presents and discusses the most likely modified DAB architecture to be practically implemented in HVDC transmission grids, based on modular multilevel converter (MMC) topology.

II. Proposed Converter

A. Converter topology

Fig.1 shows the topology of the proposed modified DAB DC/DC converter, in three phase (Fig.1(a)) and single phase (Fig.1(b)). The three phase version is advantageous relative to single phase due to its higher power handling capability, lower device ratings per phase and higher fault tolerance as continued operation is possible (with reduced power) if one phase is faulty. The AC capacitors can be connected in star or delta, as shown in Fig.1(a). For the same capacitance value per phase, delta connection can increase power transfer capability of the DC/DC converter due to the triplet effective capacitance relative to star connection. This higher effective capacitance with delta connection also means a higher filtering capability, hence harmonic content impacting AC link transformer is much lower. This suggests that delta connected capacitors can be the more favorable option, however, star connection has a key salient feature, which is the availability of the neutral point for re-balancing the system in case of unbalanced operation.

The single phase version will be used in this paper to facilitate analysis, design, operation demonstration and standardization of comparison with conventional single phase DAB. The converter comprises two bridges, each containing back-to-back switches, and the two bridges are connected via a passive CLC circuit incorporating an isolating transformer. It is worth noting, that despite the number of switching devices is double those of conventional DAB, however, at any instant of conduction only one device in the pair will be conducting with

the series diode of the other device, hence similar number of devices are in conduction.

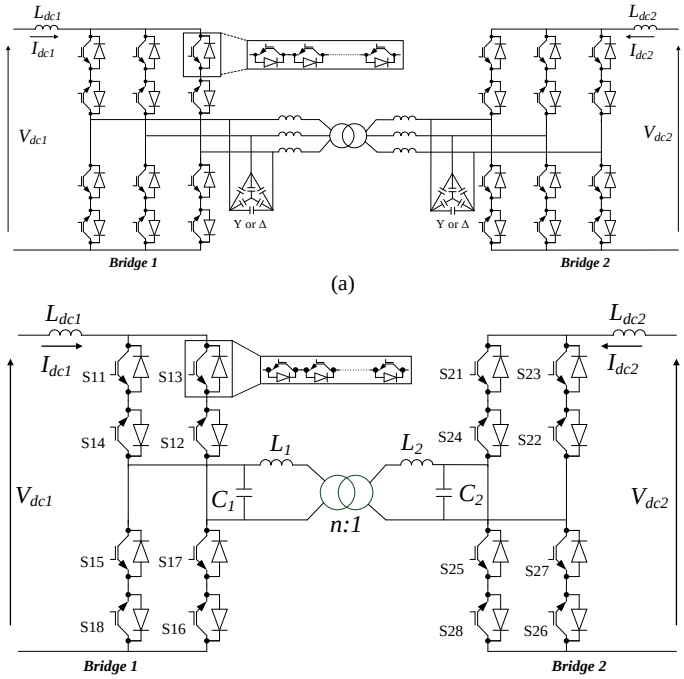


Fig.1. Proposed topology of modified DAB converter (a) three phase (b) single phase.

Although the proposed modified DAB uses the simple two-level converter technology which cascades semiconductor devices in a valve (as shown in Fig.1), however, the most likely approach of implementing this modified DAB in a practical real life HVDC system is using a MMC-based approach. Therefore, the forthcoming sections will elaborate on the analysis of the two-level topology to prove the main concept of improved efficiency and interoperability compared to conventional DAB, and the last section of the paper will present the possibility of extending this work to MMC-based approach.

B. Steady state analysis

Fig 2 shows the AC equivalent circuit of the proposed DC/DC converter. The following assumptions are made in the analysis:

- Fundamental harmonic analysis will be used as it is the main power carrier and the filtering effect of the CLC circuit provides near sinusoidal current in the inductive link.
- Transformer's magnetizing inductance is neglected.
- All transformer secondary side components are referred to the primary side using transformer turns ratio *n* (designed to match DC voltage ratio V_{dc1}:V_{dc2})
- The transformer leakage inductances on primary and secondary sides are incorporated into the main inductors L_1 and L_2 and all represented as one main equivalent inductance L.
- Lossless passive elements are used, i.e. parasitic resistances are neglected.

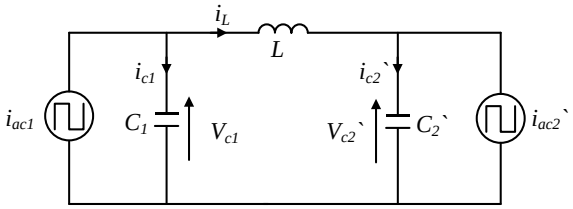


Fig. 2. AC equivalent circuit of proposed DC/DC converter.

With fundamental harmonic analysis, the circuit equations are:

$$i_{ac1}(t)=\sqrt{2}I_{ac1}\sin(\omega t),\ \overline{I_{ac1}}=I_{ac1}\angle 0 \tag{1}$$

$$i_{ac2}`(t)=\sqrt{2}I_{ac2}`\sin(\omega t-\delta),\ \overline{I_{ac2}}`=I_{ac2}`\angle -\delta \tag{2}$$

$$i_{c1}(t)=i_{ac1}(t)-i_L(t),\ \overline{I_{c1}}=\overline{I_{ac1}}-\overline{I_L} \tag{3}$$

$$i_{c2}`(t)=i_{ac2}`(t)+i_L(t),\ \overline{I_{c2}}`=\overline{I_{ac2}}`+\overline{I_L} \tag{4}$$

Where, δ is the phase shift angle between the two bridge square wave currents as depicted in Fig. 3.

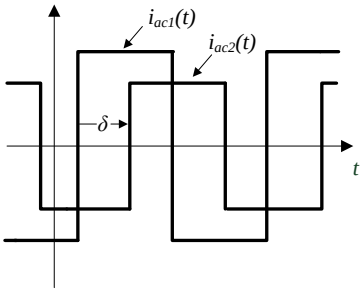


Fig. 3. Phase shift angle δ between the two bridge square wave currents.

Solving the circuit in Fig. 2 in phasor form, capacitor voltages V_{c1} and V_{c2}` can be expressed in terms of $I_{ac1}$ and $I_{ac2}$` as

$$\overline{V_{c1}}=k_1\overline{I_{ac1}}+k_2\overline{I_{ac2}}` \tag{5}$$

$$\overline{V_{c2}}`=k_3\overline{I_{ac1}}+k_4\overline{I_{ac2}}` \tag{6}$$

Where,

$$k_1=j\frac{1-\omega^2LC_2`}{\omega^3LC_1C_2`-\omega C_1-\omega C_2`}=j\frac{\alpha(\omega)}{\beta(\omega)}$$

$$k_2=k_3=j\frac{1}{\omega^3LC_1C_2`-\omega C_1-\omega C_2`}=j\frac{1}{\beta(\omega)}$$

$$k_4=j\frac{1-\omega^2LC_1}{\omega^3LC_1C_2`-\omega C_1-\omega C_2`}=j\frac{\gamma(\omega)}{\beta(\omega)}$$

$$L=L_1+L_2`,\ L_2`=n^2L_2,\ C_2`=\frac{C_2}{n^2}$$

The active power at bridge 1 can be calculated by:

$$P_{ac1}=\mathrm{Real}\left\{\overline{V_{c1}}\,\overline{I_{ac1}}^{*}\right\}=\frac{I_{ac1}I_{ac2}`}{\beta(\omega)}\sin\delta \tag{7}$$

Assuming lossless bridges, and power balance between DC and AC sides of bridge 1:

$$P_{ac1} = P_{dc1} = P = \frac{I_{ac1} I_{ac2}`}{\omega^3 L C_1 C_2` - \omega C_1 - \omega C_2`} \sin\delta \quad (8)$$

Since bridges are generating square wave AC currents from DC side currents, therefore:

$$I_{ac1} = \frac{4}{\pi}\frac{I_{dc1}}{\sqrt{2}} = \frac{2\sqrt{2}}{\pi} I_{dc1}$$

$$I_{ac2}` = \frac{4}{\pi}\frac{I_{dc2}`}{\sqrt{2}} = \frac{2\sqrt{2}}{\pi} I_{dc2}` \quad (9)$$

Substitute for AC currents in (8) yields,

$$P = \frac{8 I_{dc1} I_{dc2}`}{\pi^2 \omega\left(\omega^2 L C_1 C_2` - C_1 - C_2`\right)} \sin\delta \quad (10)$$

Substituting with $I_{dc1} = \frac{P}{|V_{dc1}|}$ and $I_{dc2}` = \frac{P}{|V_{dc2}`|}$ in (10) and re-arranging, yields the converter active power transfer relation as a function of converter parameters and operating specs,

$$P = \frac{\pi^2 |V_{dc1}||V_{dc2}`| \omega\left(\omega^2 L C_1 C_2` - C_1 - C_2`\right)}{8\sin\delta} \quad (11)$$

Where, $V_{dc2}` = nV_{dc2}$. This is the main converter power transfer equation.

C. Calculation of AC side passive elements

Values of the AC side passive elements L_1, L_2, C_1 and C_2 are calculated to ensure meeting the rated converter active power at rated frequency and DC voltages while maintaining zero internal reactive power circulation at rated active power. A generic definition of the AC currents can be given by:

$$\overline{I_{ac1}} = I_{ac1}\angle\theta_1 \,,\ \overline{I_{ac2}`} = I_{ac2}`\angle\theta_2 \,, \text{ and } \overline{I_L} = I_L\angle 0 \quad (12)$$

The active and reactive powers at bridge 1 would therefore be:

$$P_{ac1} = \frac{I_L I_{ac1}}{\omega C_1}\sin\theta_1 \quad (13)$$

$$Q_{ac1} = \frac{I_L I_{ac1}\cos\theta_1 - I_{ac1}^2}{\omega C_1} \quad (14)$$

To achieve Q_{ac1} =0 at rated power P_r and rated frequency ω_r, (13) and (14) can be manipulated to achieve:

$$C_1 = \frac{I_{ac1r}\sqrt{I_{Lr}^2 - I_{ac1r}^2}}{\omega_r P_r} \quad (15)$$

Following similar analysis for bridge 2, C_2` would be:

$$C_2` = \frac{I_{ac2r}`\sqrt{I_{Lr}^2 - I_{ac2r}`^2}}{\omega_r P_r} \quad (16)$$

Inductor L in Fig. 2 is practically split into two lump inductors in series; L_1 and L_2`. From (12), it can be deduced that both inductor voltages would be purely imaginary ($j\omega L_1 I_L$) and ($j\omega L_2` I_L$). These components can be used to counter the imaginary components of the AC capacitor voltages V_{C1} and V_{C2}`, which can be used to calculate $L_1$ and $L_2$`:

$$L_1 = \frac{P_r\sqrt{I_{Lr}^2 - I_{ac1r}^2}}{\omega_r I_{Lr}^2 I_{ac1r}} \quad (17)$$

$$L_2` = \frac{P_r\sqrt{I_{Lr}^2 - I_{ac2r}`^2}}{\omega_r I_{Lr}^2 I_{ac2r}`} \quad (18)$$

From (15)-(18), rated inductive link current I_{Lr} and bridge AC currents I_{acir} (i=1,2`) are not common name-plate specifications of the converter. The AC bridge currents are a direct function of the DC link currents (since the bridges are of current source nature), and the DC link currents are dependent on power transferred P and DC link voltages V_{dc1} and V_{dc2}. The inductive link rated current I_{Lr} is designed to reduce overall converter losses. A design ratio k will be introduced as follows:

$$k = \frac{I_{L(pk)}}{\max(I_{ac1(pk)}, I_{ac2(pk)}`)} \qquad k \geq 1 \quad (19)$$

For the purpose of analysis in this paper, this factor will be called the *current ratio*. From the aforementioned, it can be concluded that, the converter main specifications are:

- The rated power P_r
- The rated DC link voltages V_{dc1} and V_{dc2}
- The current ratio k
- The rated frequency ω_r

The AC passive elements in (15)-(18) can, therefore, be re-written as function of these main converter specifications:

$$C_i = \frac{8 P_r \sqrt{k^2 V_{dci}^2 - V_{dcLV}^2}}{\omega_r \pi^2 V_{dcLV} V_{dci}^2} \quad (20)$$

$$L_i = \frac{\pi^2 V_{dcLV}\sqrt{k^2 V_{dci}^2 - V_{dcLV}^2}}{8\omega_r k^2 P_r} \quad (21)$$

Where, i=1, 2`, $L_2 = L_2`/n^2$, $C_2 = n^2 C_2`$, LV refers to the low-voltage DC side of the converter and n is the transformer voltage ratio V_{dc1}/V_{dc2}.

D. Calculation of DC side inductors

Referring to Fig. 1, the DC side inductors L_{dc1} and L_{dc2} can be designed to control the ripple content of their respective DC currents. Assuming purely sinusoidal AC voltages across the bridge capacitors (fundamental harmonic analysis), the bridge 1 DC current ripple ΔI_{dc1} (in Amps) at rated power can be calculated using:

$$\Delta I_{dc1} = \frac{1}{\omega_r L_{dc1}} \int_{\sin^{-1}\left(\frac{2}{\pi}\right)}^{\pi - \sin^{-1}\left(\frac{2}{\pi}\right)} \left\{V_{c1pk}\sin\omega t - \frac{2}{\pi}V_{c1pk}\right\} \mathrm{d}(\omega t) = \frac{0.42}{\omega_r L_{dc1}} V_{c1pk} \quad (22)$$

From (5), the RMS value of V_{c1} can be manipulated:

$$V_{c1rms} = \sqrt{\frac{8P^2}{\pi^2\beta(\omega)^2}\left[\frac{1}{V_{dc2}`^2} + \frac{\alpha(\omega)^2}{V_{dc1}^2} + \frac{2\alpha(\omega)\cos\delta_r}{V_{dc1} V_{dc2}`}\right]} \quad (23)$$

Where, δ_r is the phase shift angle between the AC bridge currents at rated power, calculated from rated power equation (11). Therefore, the peak voltage (assuming sinusoidal waveform) is:

$$V_{c1peak} = \frac{4P\sqrt{V_{dc1}^2 + \alpha(\omega)^2 V_{dc2}^2` + 2\alpha(\omega)V_{dc1}V_{dc2}`\cos\delta_r}}{\pi|\beta(\omega)|V_{dc1}V_{dc2}`} \quad (24)$$

Substituting (24) into (22), and manipulating, L_{dc1} could be obtained as a function of percentage ripple current (percentage of the main current I_{dc1}):

$$L_{dc1} = \frac{168\sqrt{V_{dc1}^2 + \alpha(\omega)^2 V_{dc2}^2` + 2\alpha(\omega)V_{dc1}V_{dc2}`\cos\delta_r}}{\pi\omega_r|\beta(\omega)|\Delta I_{dc1(\%)}V_{dc2}`} \quad (25)$$

Where, $\Delta I_{dc1(\%)} = \Delta I_{dc1}$ x $100/I_{dc1}$. Applying similar analysis to bridge 2 yields:

$$L_{dc2}` = \frac{168\sqrt{V_{dc2}^2` + \gamma(\omega)^2 V_{dc1}^2 + 2\gamma(\omega)V_{dc1}V_{dc2}`\cos\delta_r}}{\pi\omega_r|\beta(\omega)|\Delta I_{dc2(\%)}V_{dc1}} \quad (26)$$

Where, $L_{dc2} = L_{dc2}`/n^2$ and $\Delta I_{dc2(\%)} = \Delta I_{dc2}$ x $100/I_{dc2}$.

III. Design Procedure and Performance Analysis

The full design procedure of the converter components follows these steps:

1. Depending on the DC system where the DC/DC converter would be operating, main converter specifications would be given: rated DC voltages V_{dc1} and V_{dc2} and rated power P_r.
2. Select main converter design parameters: current ratio k and rated base frequency ω_r (basis of selection to be analyzed).
3. Calculate AC circuit parameters L_1, L_2, C_1, and C_2 from (20) and (21).
4. Calculate rated phase shift angle δ_r from (11).
5. Calculate DC link inductors L_{dc1} and L_{dc2} from (25) and (26) with pre-defined current ripple requirements.

Step 2 above is the main step in the converter design procedure. It involves the careful selection of two main parameters (k and ω_r) which would affect converter component sizing and operational performance. The selection of these parameters is crucial and cannot be arbitrary. The effect of these two parameters will be analyzed on:

- Peak capacitor voltages (V_{c1pk} and V_{c2pk}) as this affects peak voltage stresses on switching devices.
- Peak inductor current (I_{Lpk}).
- Passive elements sizing.
- Overall converter efficiency at rated power.

Optimum value will be selected for the two parameters (k and ω_r) based on this analysis. To benchmark this analysis and make it more meaningful, a comparison is made with conventional DAB converter. Both converters are compared on a per unit basis, to make the analysis generic and non rating-specific. Base values chosen are V_{dc1} as base voltage at transformer primary side, V_{dc2} at transformer secondary side and rated power P_r as base power.

For a given set of converter specifications (V_{dc1}, V_{dc2} and P_r), analysis is performed varying the two design parameters (k and ω_r) for the proposed converter and solely ω_r for conventional DAB as the *current ratio* parameter does not exist. The steady state analysis in section II will be used for this purpose. Efficiency at rated power is calculated in both converters considering the following:

- Switching devices used for loss calculations are the ABB StakPak 4500V, 2000A IGBT module 5SNA2000K451300.
- The dominant IGBT loss is the conduction loss since at rated power conventional DAB operates in ZVS mode due to lagging inductor current and proposed converter operates in ZCS due to zero bridge reactive power (unity power factor). This means that switching loss effect is minimal and would therefore be neglected.
- Due to the ZCS and ZVS operation in the proposed and conventional DAB respectively, simple lossless snubbers can be used, hence snubber circuit losses are negligible.
- Number of series IGBTs stacked in the valve is calculated dependent on peak voltage stresses.
- DC inductor parasitic resistance is selected at an empirical value of 0.005pu. AC inductor parasitic resistance is considered slightly higher (0.015pu) to account for skin effect.
- AC capacitor ESRs are considered for proposed converter at an empirical value of 0.001pu.
- Transformer core losses are estimated for both proposed and conventional DAB converters allowing for eddy current and hysteresis losses based on an adaptation of Steinmetz formula [22],

$$P_{core} = C_m f^{\alpha} B_m^{\beta} \quad (27)$$

Where, C_m, α and β are real empirical parameters, f is the fundamental AC frequency and B_m is the max core flux density dependent on the max inductive link current $I_{L(pk)}$.

Fig. 4 shows the effect of varying k and ω_r for the two converters (conventional and modified DAB). The rated frequency ω_r will be displayed in per unit on a base medium frequency of 500Hz. Fig. 4(a) shows that the efficiency of conventional DAB is independent of k (where this is not a design factor), and degrades with increasing frequency. Efficiency of proposed converter degrades at high current ratios k due to increasing current $I_{L(pk)}$ with k (See Fig.4(b)). The cutoff value for selection of current ratio to ensure higher efficiency in proposed converter is k=1.5, where beyond that inductive link current increases significantly and efficiency falls. Reduction in efficiency of proposed converter with frequency increase is almost negligible, which presents a significant advantage over its counterpart. Therefore, the maximum value of ω_r =1 pu will be utilized to ensure minimum passive component sizing (see sizing of L in Fig. 4(b)).

Since operation at maximum possible efficiency is the primary design target, therefore the optimum selection of the current ratio design factor is approximately at k=1.2. At this value, the peak AC capacitor voltages are rated at 2.2pu as shown in Fig. 4(b), meaning that IGBTs will experience a worst-case peak of 2.2 times the DC link voltage. These are considered worst-case values as they are calculated using the undamped (lossless) analysis in section II. As hypothesized, boosted AC capacitors' voltages contributed in reducing current in the proposed converter, which reduced losses compared to conventional DAB and boosted efficiency. Fig. 5 shows efficiency comparison at the selected optimal operating conditions (k=1.2 and ω_r=1 pu) and detailed losses breakdown of both modified

and conventional DAB converters. It can be concluded that the main loss components causing the higher losses in the conventional DAB are the AC inductor and transformer core losses. These have been significantly reduced in the modified DAB, thanks to the reduction in inductive link current.

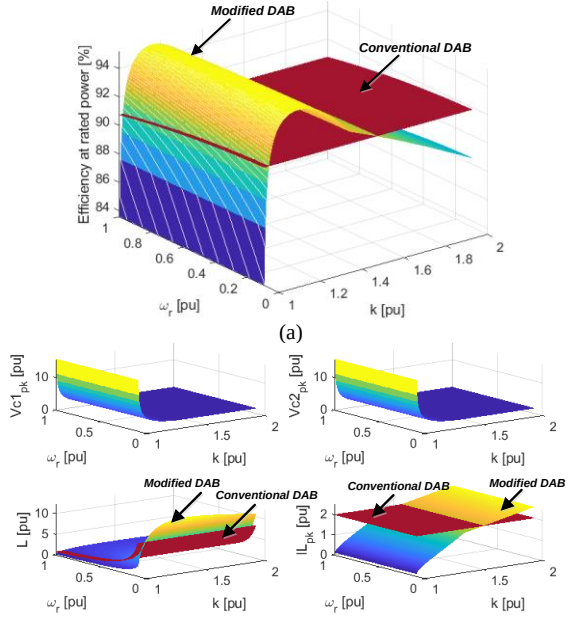


Fig. 4: The effect of varying current ratio k and ω_r in conventional and modified DAB at rated power and rated voltages (a) Efficiency at rated power (b) Various converter parameters and components.

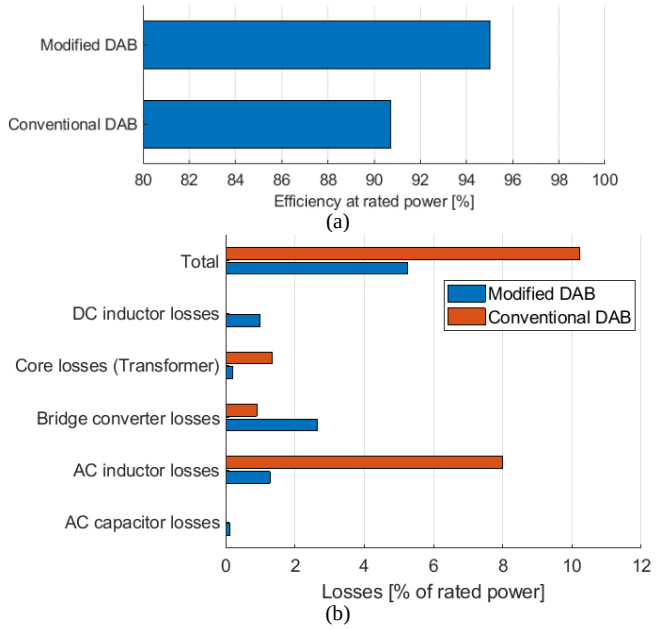


Fig. 5: Comparison between the modified and conventional DAB converters at optimal selected k and ω_r (a) Efficiency at rated power (b) Losses breakdown.

IV. Time Domain Simulations

This section presents the Matlab/Simulink time domain simulation modeling of the proposed DC/DC converter under different operating scenarios. The system parameters are listed in Table 1, with design based on optimal efficiency achieved from selection in section III (k=1.2 and ω_r =1pu at base frequency of 500 Hz).

Table 1: Simulation test system parameters

Rated power P_r	200MW
High voltage DC side voltage V_{dc1}	160kV
Low voltage DC side voltage V_{dc2}	80kV
Rated frequency f_r	500 Hz
Current ratio k	1.2

For the sake of comparison with conventional DAB, both converters will be designed to the system ratings in Table 1, with the exception of the current ratio which does not exist for conventional DAB. The component parameters and ratings are selected according to the detailed procedure in section III and are listed in Table 2.

Table 2: Converter component parameters and ratings

	Modified DAB	**Conventional DAB**
AC capacitor C_1	1.26µF, 180kV(RMS)	
AC capacitor C_2	5.05µF, 90kV (RMS)	
Transformer	200MVA, 180/90kV, 500Hz, X=10%	200MVA, 160/80kV, 500Hz, X=10%
AC inductor L_1	20.6mH, 1328A (RMS)	14mH, 2041A (RMS)
AC inductor L_2	5.1mH, 2656A (RMS)	3.5mH, 4082A (RMS)
DC inductor L_{dc1}	500mH, 1250A (7.5% ripple)	
DC inductor L_{dc2}	125mH, 2500A (7.5% ripple)	
DC inductor parasitic resistance (0.005pu)	R_{dc1}=0.64Ω R_{dc2}=0.16Ω	
AC inductor parasitic resistance (0.015pu)	R_{L1}=1.92Ω R_{L2}=0.48Ω	R_{L1}=1.92Ω R_{L2}=0.48Ω
AC capacitor ESR (0.001pu)	R_{C1}=0.128Ω R_{C2}=0.032Ω	

A. Converter connecting two VSC HVDC lines

Fig. 6 shows simulation results for the proposed DC/DC converter steady state operation at the rated 200 MW power. The DC side currents I_{dc1} and I_{dc2} in Fig. 6(a) show active power transferred from bridge 1 to bridge 2. The peak capacitor voltages V_{c1pk} and V_{c2pk} are less than the worst-case peak of 2.2 pu outlined in the analysis in section III. V_{c1} and I_{ac1} are in phase indicating almost zero reactive power and positive active power at bridge 1 as in Fig. 6(b). V_{c2} and I_{ac2} are 180º (out of phase) to indicate negative power at bridge 2 and zero reactive power as in Fig. 6(c). The phase angle difference δ between I_{ac1} and I_{ac2} is δ =-116º confirming the power transfer in (11) of 200 MW. This is the ideal power transfer assuming the lossless analysis leading to (11). Practically, the DC side powers calculated from the DC voltages and currents in Fig. 6(a) are 202 MW and 192 MW at bridge 1 and 2 respectively, with conversion efficiency 95.2%. This confirms the theoretical modified DAB efficiency given in Fig. 5(a). Finally, it can be noted that the peak inductive current I_{L1pk} is 1.2 times the peak fundamental current of I_{ac1} confirming the design factor k=1.2.

To confirm the successful operation of the proposed DC/DC converter with bi-directional power flow, Fig. 7 illustrates the

transient behaviour during power reversal at rated loading. The converter operates initially with forward power flow (from bridge 1 to bridge 2), then at t=3s, power flow is reversed. The converter can inject power in both directions smoothly between the two terminals. Voltages are with fixed polarities and currents changes polarities at both bridges in complementary manner.

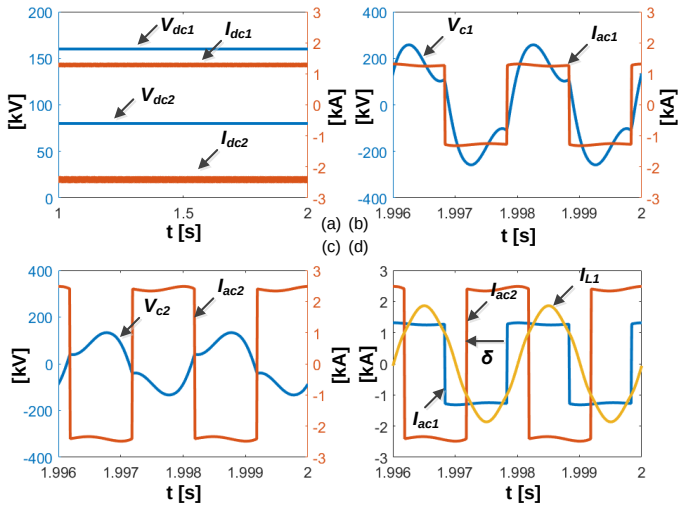


Fig. 6: Steady state simulation results at rated power and rated voltages connecting two VSC-HVDC lines (a) DC link current/voltage waveforms, (b) Bridge 1 AC side current/voltage waveforms, (c) Bridge 2 AC side current/voltage waveforms, and (d) Both AC bridge currents and the inductor current including the phase shift (δ) control.

Fig. 8 shows results for the case of a pole-to-pole DC fault at bridge 1 DC side. Full rated power is being sourced from bridge 2 when the permanent fault is applied at t=1.5s. V_{dc1} drops to zero due to the bolted fault as in Fig. 8(a) and the current I_{dc1} remains at 1pu, while I_{dc2} is almost zero highlighting the inherent fault isolation characteristic of the converter without any external control or semiconductor tripping. Due to the power balance phenomenon, the converter acts as a fault isolator between both DC sides preventing propagation of DC fault effect. Fault side current I_{dc1} remains at full-load during the fault due to operation of fault side AC circuit purely in reactive power mode. This can be confirmed from the 90º phase shift of V_{c1} and I_{ac1} (purely capacitive operation) as in Fig. 8(b). V_{c2} is almost purely sinusoidal as the current passing through C_2 is the sinusoidal inductor current since I_{ac2}=0 as in Fig. 8(c).

B. Converter connecting LCC and VSC HVDC lines

In this sub-section, an LCC-HVDC is connected to VSC-HVDC line via the proposed DC/DC converter. Steady state simulation results are shown in Fig. 9 when the power is sourced from bridge 2 (VSC-HVDC) to bridge 1 (LCC-HVDC). V_{dc1} is with bidirectional polarity as it is connected to LCC-HVDC with its negative voltage capability, while V_{dc2} is unipolar as it is connected to VSC-HVDC as in Fig. 9(a). For the currents, I_{dc1} is unipolar and I_{dc2} is bidirectional depending on the power flow. V_{c1} and I_{ac1} are 180º out of phase to indicate negative power at bridge 1 and zero reactive power as in Fig. 9(b). V_{c2} and I_{ac2} are in phase indicating zero reactive power and positive power at bridge 2 as in Fig. 9(c). The phase angle difference δ between I_{ac1} and I_{ac2} is δ =116 confirming the power transfer of 200MW from (11) as in Fig. 9(d).

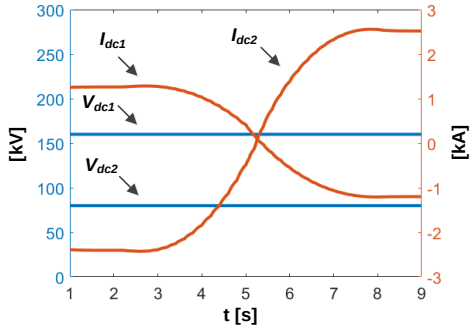


Fig. 7: Transient power reversal for connecting two VSC-HVDC lines.

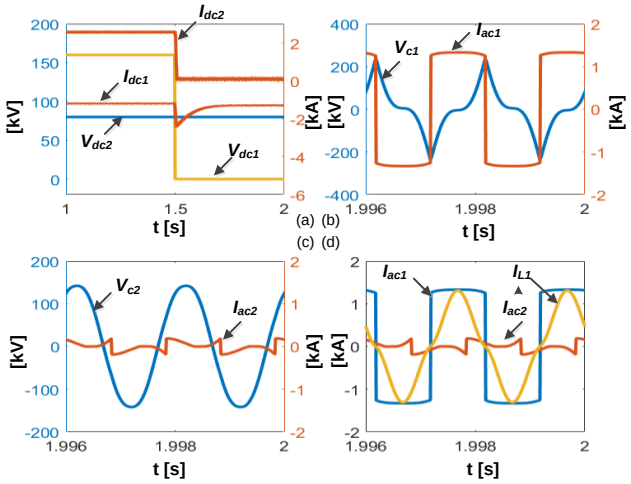


Fig. 8: Simulation results for a pole-to-pole DC fault at bridge 1 connecting two VSC-HVDC lines.

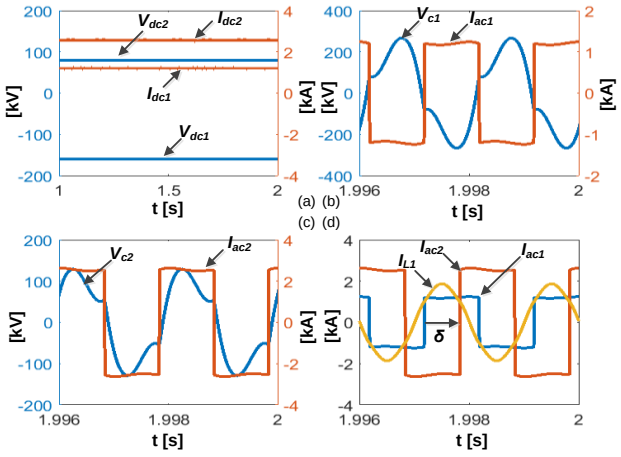


Fig. 9: Steady state simulation results at rated power and rated voltages connecting VSC-HVDC to LCC-HVDC.

Fig. 10 shows the transient behavior of the converter during power reversal at rated loading. At bridge 1, V_{dc1} changes its polarity and I_{dc1} remains unipolar as thyristorized LCC-HVDC systems can only operate with unipolar DC link current. At bridge 2, V_{dc2} has fixed polarity, and I_{dc2} changes its polarity to realize power reversal.

Fig. 11 shows results for the case of a pole-to-pole DC fault at bridge 1 (LCC-HVDC) DC side. Full rated power is being sourced from bridge 2 when the permanent fault is applied at t=1.5s. It can be seen when V_{dc1}=0, current at bridge 2 falls to zero (I_{dc2}=0) as in Fig. 11(a), showing similar fault isolation characteristic as illustrated earlier. The effect of faults in the AC link is also studied with a short circuit fault applied across the AC terminals of bridge 2 (or across capacitor C_2) while it is receiving rated power from bridge 1. Results shown in Fig.12 reveal that when the fault is applied at C_2 at t=1.5s, V_{c2} drops to zero and the through-path for current to DC side of bridge 2 is interrupted. This pulls down I_{dc2} and I_{ac2} to zero ceasing power transfer. Bridge 1 (connected to the LCC-HVDC) rides through the fault and regulates I_{dc1} to rated value (1250A) by reducing DC link voltage V_{dc1} to approximately 10kV. Since the equivalent impedance seen from AC terminals of bridge 1 is purely reactive, V_{c1} and I_{ac1} are 90˚ out of phase. I_{L1} is the fault current passing through the AC inductors and transformer which is 35% higher than rated value of I_{L1} in Fig. 9.

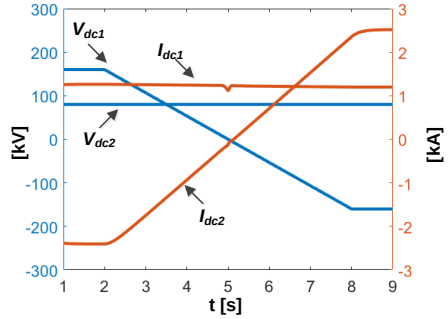


Fig. 10: Transient power reversal for connecting VSC-HVDC to LCC-HVDC.

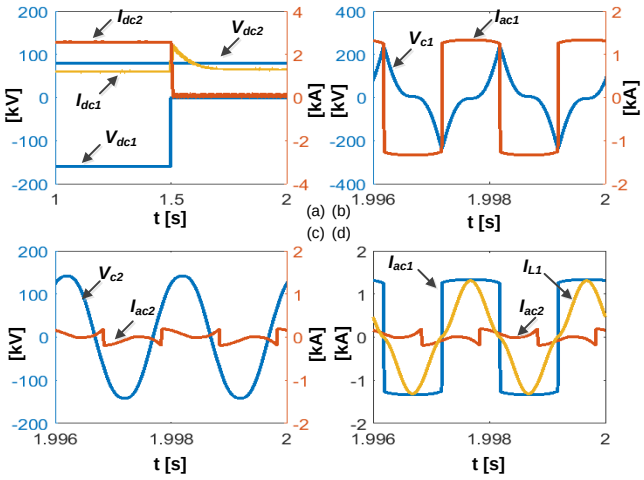


Fig. 11: Simulation results for a pole-to-pole DC fault at bridge 1 (LCC-HVDC) connecting VSC-HVDC to LCC-HVDC.

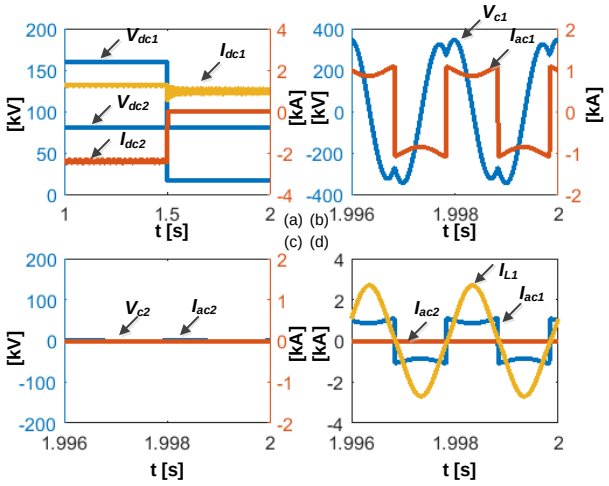


Fig. 12: Simulation results for an AC fault at AC terminals of bridge 2 (across capacitor C_2) connecting VSC-HVDC to LCC-HVDC.

The converter has a stable response to AC link faults and while bridge 1 rides through the fault by appropriate external regulation of LCC-HVDC voltage, bridge 2 isolates the fault by DC current dropping to zero due to natural power balancing.

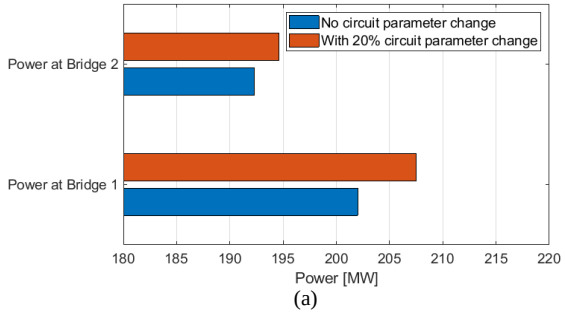
C. Sensitivity analysis

In order to assess the sensitivity of the proposed design to circuit parameter variations, 20% change in the passive circuit parameters L_1, L_2, C_1 and C_2 will be applied. The effect of this parameter change on the rated power transferred (from bridge 1 to bridge 2) and resulting conversion efficiency is depicted in Fig. 13. Due to this parameter change:

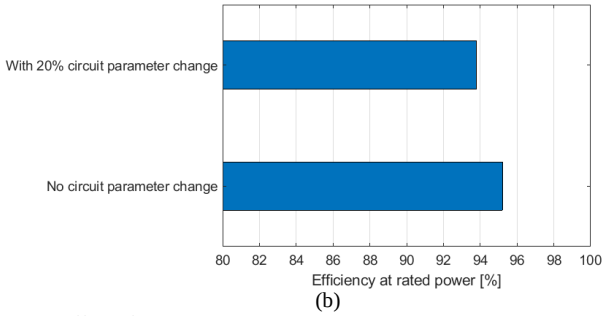
- The overall conversion efficiency dropped from 95.2% to 93.8% representing a change of 1.4%.
- The change in power sent from bridge 1 is 2.7%.
- The change in power received at bridge 2 is 1.2%.

This shows that the 20% simultaneous change in the four circuit parameters has caused only minor changes to converter efficiency and power transfer capability which confirms the robustness of the proposed converter design procedure.

In addition, the reduced efficiency after the circuit parameter change (93.8%) is still higher than conventional DAB efficiency (90.7%) shown in Fig. 5(a). This shows that even with the assumed circuit parameter change, the performance of the modified DAB is superior to the conventional DAB.



(a)



(b)

Fig. 13: Effect of circuit parameter variation on: (a) Power at bridge 1 and 2 (b) Conversion efficiency.

V. Experimental Validation

A lab-scale prototype of the proposed DC/DC converter, depicted in Fig. 14, is used to validate the time-domain performance in section IV. A 32-bit Cypress microcontroller (CY8CKIT-050 PSoC® 5LP) is used for the gate switching. The test rig system parameters are presented in Table 3.

Table 3: Experimental system parameters

Rated power P_r	400W
High voltage DC side voltage V_{dc1}	100V
Low voltage DC side voltage V_{dc2}	50V
Rated frequency f_r	500 Hz
High voltage side AC capacitance C_1	6.8µF
Low voltage side AC capacitance C_2	27.4µF
Transformer total leakage inductance (referred to HV side)	9mH

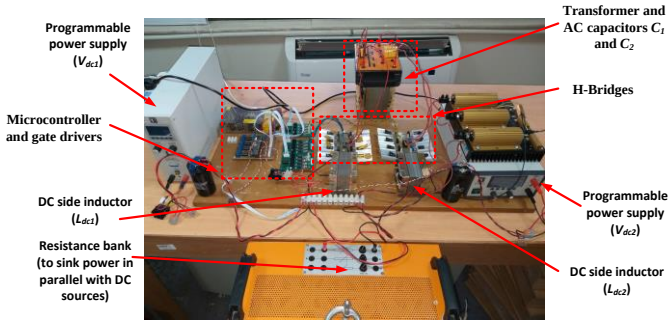


Fig. 14: Experimental test rig

Results for connecting the proposed DC/DC converter to two VSCs are shown in Fig. 15, where steady state DC side currents and voltages in Fig.15(a) show reverse power flow operation (bridge 2 to bridge 1). The AC link results in Fig. 15(b) show in-phase voltages and currents at bridge 2 an out-of-phase voltages and currents at bridge 1 corresponding to the reverse power flow case in Fig. 15(a) and highlighting the almost-zero reactive power operation at the rated 400W. Bolted DC fault is applied for 150ms at bridge 1 in Fig. 15(c) showing how bridge 2 current I_{dc2} responded by dropping to almost zero, isolating the fault and preventing its propagation. The converter restores normal operation after fault clearance. Fig. 15(d) depicts the transient reversal of rated power by reversing current polarities at both bridge DC sides.

Fig. 16 displays similar results for using the proposed DC/DC converter to connect LCC and VSC. The main difference is noted in reverse power flow being achieved using inverse voltage polarity at bridge 1 connected to LCC rather than inverse current polarity.

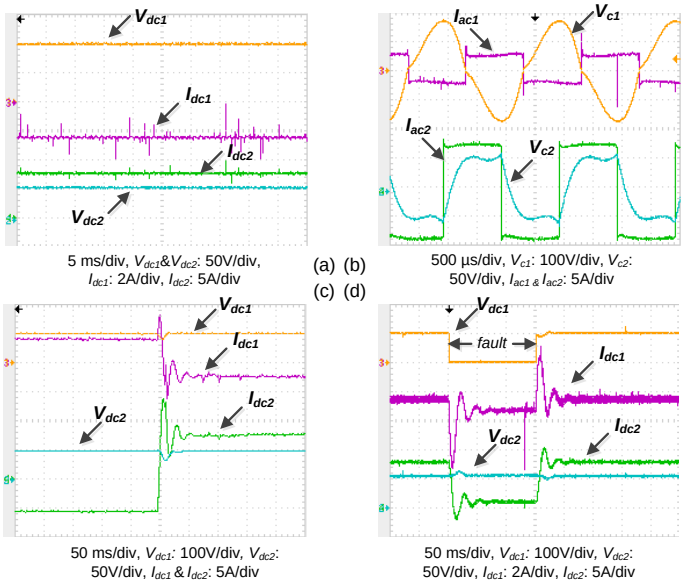


Fig. 15: Experimental results for proposed DC/DC converter connecting two VSCs (a) Steady state DC link current/voltage waveforms, (b) Steady state AC side current/voltage waveforms, (c) Transient power reversal, and (d) Pole-to-pole DC fault at bridge 1.

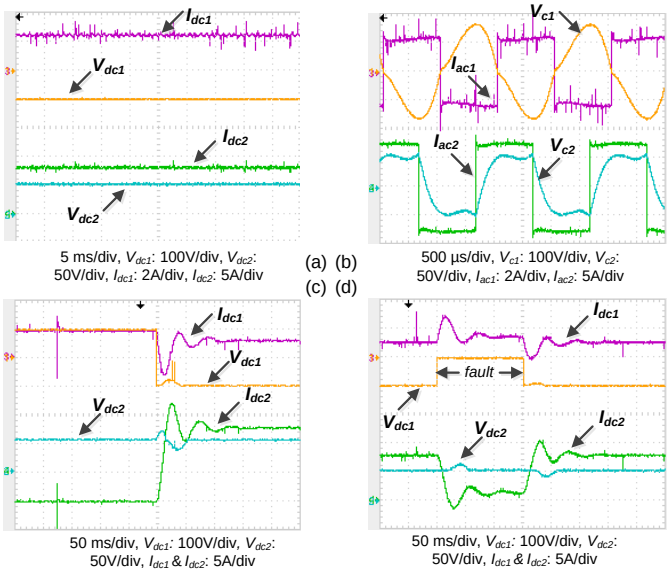


Fig. 16: Experimental results for proposed DC/DC converter connecting LCC and VSC (a) Steady state DC link current/voltage waveforms, (b) Steady state AC side current/voltage waveforms, (c) Transient power reversal, and (d) Pole-to-pole DC fault at bridge 1 (LCC side).

VI. Modular Converter Topology

Modular multilevel converters (MMCs) are becoming increasingly popular in VSC-based HVDC projects commis-

sioned recently. This is due to their desirable operating features including modular structure with low-power sub-modules, avoidance of semiconductor devices series connection, lower semiconductor switching losses, better output power quality and lower *dv/dt* stresses on transformers. The modified DAB in this paper generates rectangular AC currents which have *di/dt* that create high voltage transients during switching. It is possible to implement the proposed modified DAB in a modular approach, similar to typical MMC topology, to exploit the aforementioned advantages it offers, and make it more appropriate for HVDC transmission. Fig.17 depicts the modular topology for the proposed modified DAB.

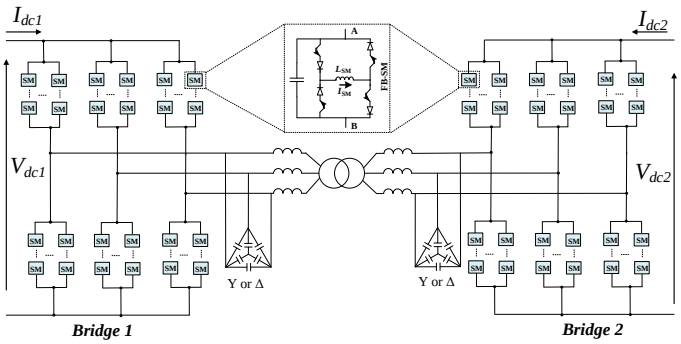


Fig. 17: MMC-based topology for the proposed modified DAB

Since bridges 1 and 2 in the proposed DAB operate in current source mode generating AC currents, the MMC bridges would have to be designed to shape their output AC current rather than the voltage. Therefore, the topology would have to exploit the duality circuit theory between current and voltage source converters. The dual current source MMC topology has been presented in [23], and is applied here to the proposed DC/DC converter in Fig.17. Sub-modules (SMs) are constructed of full-bridge cells with a DC inductor as the main storage element and an AC capacitor for voltage sharing among series SMs [24]. The SM DC inductors replace the bulky DC link inductors in the two-level topology. The SM capacitors should be AC to cater for typical bipolar voltages occurring during power reversal in current source converters. The SMs are connected in parallel and SM inductor current balancing is maintained using appropriate switching algorithms similar to voltage balancing techniques in voltage source MMCs. The full-bridge cells are important to ensure bi-directional current flow capability in the cells to enable power reversal via DC link current change of polarity. To realize this, the IGBTs are in common emitter configuration to allow for unipolar current in the inductor storage element while current between SM terminals A/B being bipolar. The series diodes block negative SM capacitor voltages.

CONCLUSION

In this paper, a modification has been presented to the standard dual active bridge DC/DC converter topology to improve its efficiency and allow interoperability in hybrid LCC/VSC HVDC transmission grids. The hypothesis was based on adding AC capacitors at the H-bridge outputs to boost AC link voltages to reduce currents for the same level of power transferred. This modification had manifold benefits including, the possibility of reactive power compensation in the AC link to further reduce currents, allowing unity power factor operation with ZCS, and changing the converter H-bridges to operate in current source mode to enable interoperability of those H-bridges with LCC and VSC converter technologies. The latter feature will present a significant advantage in future meshed DC grids where interfaces between LCC and VSC are high likely; an issue which is particularly challenging in power reversal. Detailed converter design, component selection procedure and loss analysis has been presented which confirmed the initial hypothesis, and time domain simulations together with an experimental low scale prototype substantiated the various features and operating modes of the proposed converter. It has also been shown that the idea of the proposed converter is feasible for implementation using MMC-based approach which is the more practical topology for HVDC transmission.

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